

REMARKS

Applicants elect, without traverse, to have the invention of Group I, Claims 1-15 and 23-25 examined. Claims 16-22 and 26-29, which are drawn to the invention of Group II, are canceled without prejudice.

Claim 23 has been amended for purposes of clarity and thus for reasons unrelated to patentability.

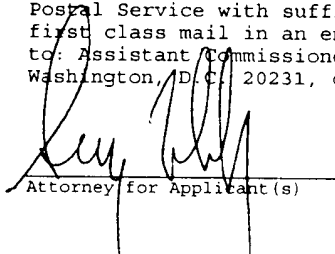
New Claims 30-40 have been added. Support for Claims 30-40 appears in the specification at least at page 5, line 33 to page 10, line 36 and in FIGS. 1, 2, and 3.

CONCLUSION

Claims 1-15, 23-25, and 30-40 are pending in the application. If the Examiner has any questions relating to the above, the Examiner is respectfully requested to telephone the undersigned Attorney for Applicant(s).

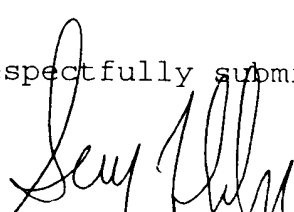
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Attorney for Applicant(s)

April 4, 2003
Date of Signature

Respectfully submitted,


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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Thomas P. Glenn et al.
Assignee: Amkor Technology, Inc.
Title: WAFER HAVING BACK-SIDE ALIGNMENT MARKS
Serial No.: 09/803,084 Filed: March 8, 2001
Examiner: Williams, Group Art
Alexander O. Unit: 2826
Docket No.: G0049

Monterey, CA
April 4, 2003

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

Claims 16-22 and 26-29 have been cancelled without prejudice.

Claim 23 has been amended as follows:

23. (AMENDED) A wafer comprising:
a first surface;
a second surface;
a scribe grid coupled to said first surface; and
a plurality of alignment marks extending from said first surface to said second surface, said plurality of alignment marks having a positional relationship to said scribe grid.

New Claims 30-40 have been added as follows:

30. (NEW) The wafer of Claim 2 wherein said scribe grid comprises an etched silicon oxide layer.

31. (NEW) The wafer of Claim 23 wherein said scribe grid comprises an etched silicon oxide layer.

32. (NEW) The wafer of Claim 23 further comprising electronic components delineated by said scribe grid.

33. (NEW) The wafer of Claim 32 wherein said electronic components are selected from the group consisting of integrated circuits, micromachine chips and image sensor chips.

34. (NEW) The wafer of Claim 32 wherein said electronic components comprise bond pads coupled to said first surface.

35. (NEW) The wafer of Claim 32 wherein said electronic components comprise active areas coupled to said first surface.

36. (NEW) The wafer of Claim 25 wherein said vertical scribe line extends in a first direction and wherein said horizontal scribe line extends in a second direction, said wafer further comprising a flat extending in said second direction.

37. (NEW) A wafer comprising:
a front-side surface;
a back-side surface;
a first scribe line coupled to said front-side surface;
and
a first back-side alignment mark extending from said front-side surface to said back-side surface, said first back-side alignment mark being formed along said first scribe line.

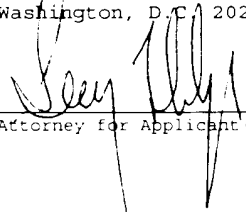
38. (NEW) The wafer of Claim 37 further comprising a plurality of back-side alignment marks extending from said front-side surface to said back-side surface, said plurality of back-side alignment marks comprising said first back-side alignment mark.

39. (NEW) The wafer of Claim 38 wherein said plurality of back-side alignment marks have a positional relationship to said first scribe line.

40. (NEW) A wafer comprising:
a first surface;
a second surface;
a scribe line coupled to said first surface; and
a means for determining a position of said scribe line
from said second surface, said means for determining extending
through said wafer from said first surface to said second
surface.

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